

Single Input Double Output DC-DC Converter Topology Using a Band-stop Filter

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Abstract- The rapid technological revolution has drastically increased global electrical energy demand, particularly for modern DC-powered electronic devices and renewable energy sources such as photovoltaic systems. Achieving appropriate voltage levels in these applications relies heavily on DC–DC converters; however, as systems increasingly require multiple voltage outputs, using several converters becomes inefficient, leading to the development of single-input multiple-output structures. This paper introduces a new single-input double-output (SIDO) DC–DC converter topology that employs a mixed structural approach and incorporates a band-stop filter, adapted from communication electronics, to generate two stepped-down DC output voltages. The operating modes and switching states of the proposed converter are analysed, and a full mathematical model is developed using the state-space method. MATLAB/Simulink simulations are conducted based on a realistic application scenario to assess performance. Cross-regulation behaviour and output isolation are examined to evaluate stability and independence between the two outputs. Simulation results show that the converter delivers two regulated voltages with significantly reduced ripple—improving from 3% to 1.83% for the 12 V output and from 14% to 3% for the 5 V output—while maintaining an overall efficiency of 93.27%. These findings demonstrate the effectiveness of the proposed topology and highlight its potential advantages over existing multi-output converter designs in terms of performance, practicality, and ripple suppression.

Keywords DC-DC converter, tank circuit, cross regulation, emerging technology.

1. Introduction

Throughout history, humanity has experienced several revolutions that led to the current state of technological advancement. Due to that, the world economy has prospered, and the life standards have risen drastically where some aspects of life that are considered normal now used to be absent a hundred years ago [1]. With this development, global problems such as pollution energy production and its efficiency are becoming more grievous [2-3]. New solutions for such problems are being introduced every day leading to a new trend based on renewable and green energy which popularity has vastly increased in the recent years [4-6]. This trend led to the development of new power electronic devices, especially DC-DC converters, to support, power and regulate

this technology [7-8]. However, DC-DC converters with a single output are no longer sufficient to supply modern devices as they need more than one single voltage level to operate [9]. These DC-DC converters can be classified into isolated and non-isolated converters depending on the presence and absence of a transformer respectively [10]. But the presence of the transformer has several disadvantages mainly on the bulkiness and efficiency of the converter [11], so the non-isolated will be the one under the scope of this study. Such converters are used in on-chip power supplies [12], consumer electronics [13-15], renewable energy applications [16-18] and electric vehicle applications [19-20].

Renewable energy is the most important among the applications mentioned above. Not only does it reduce

pollution, but also supplies the power required for the other applications to function [21]. So, efforts were made to develop all the technologies related to renewable energy [22].

And since DC-DC converters are a vital component for renewable energy to function [23], making new topologies for DC-DC converters is considered a step forward in advancement.

Reference [24] presents a single input multi output (SIMO) converter that uses a single inductor to get stepped up, stepped down, and inverted outputs all at the same time. This topology uses only one inductor which has several advantages. However, this topology uses a relatively high number of switches which will have a negative effect on the efficiency especially for high power applications.

In [25], the mix-match method was used to combine the boost topology with other topologies like the CUK and SEPIC topologies to get multiple outputs. This topology reduces the number of switches used which enhances efficiency, but at the same time it sacrifices the controllability of one of the present outputs. This means that only one output can be regulated in this topology, hence, this topology suffers from a severe case of cross-regulation.

[26] presents a single input multiple DC-DC converter topology. This topology was simulated and implemented, where it gave good results in terms of stability and efficiency. However, in this topology the two subparts of the simulated converter are directly connected to the supply which might increase the average voltage stress on the switches which might affect their lifetime.

In this paper, a new topology of SIMO converters is proposed to tackle the two problems facing the topologies studied in [24] and [25]. This topology uses the mix-match approach that is used in [25] to combine two buck converters to get two different outputs, but at the same time, it contains two switches instead of one, solving the cross-regulation problem. At the same time, this topology uses the same number of switches as the number of outputs in the converter which gives it a perfect balance between controllability and efficiency. Add to this that the switches in the proposed topology are placed in a cascaded manner which decreases the voltage stress on the switches, especially the second one. This topology uses a band-stop filter to connect the two outputs to the same input while preventing any interference between them. Moreover, this topology can handle enough power not only to be used in modern electronic devices but also to be used in renewable energy applications.

Section 1 consists of the introduction to the topic. Section 2 explains the proposed circuit, its design rules and its mathematical model. Section 3 contains the MATLAB/Simulink simulation of the proposed circuit, the simulation results and a simulated comparison between the proposed circuit and another circuit present in the literature.

And finally, section IV contains the conclusion for the whole study.

2. Proposed Circuit

The circuit of the proposed topology is shown in Fig. 1. This circuit uses a modified mix-match approach to combine two buck converters into a single multiport converter. There are several issues that should be tackled while designing single input double output (SIDO) converter, mainly cross regulation, and the interference between the two outputs of the converter [10], [26]. These two problems were tackled and successfully solved in the proposed topology. The proposed topology working principle is similar to that of a buck converter, the first switch Q1 chops the input voltage for output port V1, while switch Q2 chops the voltage coming from Q1 for output port V2. The band stop filter will be designed to filter a certain frequency to isolate the two outputs, hence the switching frequency of the two switches should be different, the only constraint is that the switching frequency of Q2 should be higher than that of Q1. The placement of the switches Q1 and Q2 as shown in Fig.1 solves the cross-regulation problem with the condition of having V1 higher than V2. This placement also simplifies modeling and controlling this circuit since it reduces the number of states of operation of this topology to only three states. Diodes D1 and D2 are placed in such a way to stop the interference coming from V2 to V1 and from V1 to V2 respectively. However, the goal is to have complete isolation between the two outputs, so additional actions should be taken. Figure 2 shows the circuit of the band-stop filter topology used in this study. A band-stop filter is a filter that filters out a certain frequency out of the spectrum while leaving all other frequencies mostly intact [27]. The simplicity of this circuit and its functionality has given it a place in the proposed topology. The band-stop filter used, capacitor C1 and inductor L1, will filter out the frequency used for switching Q2 while leaving all the other frequencies like the one used for controlling switch Q1 intact, hence preventing interference coming from that side. The higher voltage output port suffers from the greatest noise and interference problems due to the placement of its branch between two switches. With the addition of the band-stop filter, the noise and interference affecting this branch, which mainly comes from Q2 will be filtered out leaving only the clean and useful pulse width modulation frequencies to reach the output. Capacitors C2 and C3, inductors L2 and L3, and diodes D3 and D4 all can be designed based on the same principles of a conventional buck converter due to the similar configuration. The same goes for duty cycle calculation, where the duty used to control Q1 is calculated based on the output voltage V1 while that of Q2 can be calculated based on the output voltage V2.

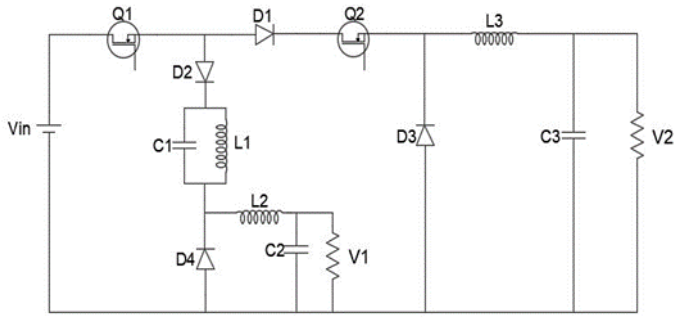


Fig. 1. The circuit of the proposed topology.

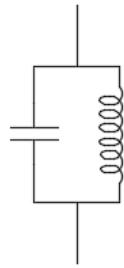


Fig. 2. Band-stop filter.

2.1. Modes of Operation

The three modes of operation of the proposed circuit are given in Table 1. It shows that there are three modes of operation in this topology. Usually for a circuit with two independent switches, there would have been 4 modes of operation but the placement of switches S1 and S2 reduces that to only 3 modes because the mode where S1 is off and S2 is on has become unrealistic due to the fact that not only it fails to charge any components in this state due to the source being disconnected, but also due to the fact that it increases the chance of the two outputs to interfere with each other.

Table 1. Modes of operation of the proposed topology

	Q1	Q2
d1	ON	ON
d2	ON	OFF
d3	OFF	OFF

Figure 3a shows the circuit in mode **d1**; both switches are conducting, diodes D1 and D2 are conducting while diodes D3 and D4 are reversed biased. C2, C3, L2 and L3 are being charged and both outputs are being supplied by the main supply.

Figure 3b depicts the circuit in operation mode **d2**. Switch 1 is still on while switch 2 has been turned off. In this mode, diodes D2 and D4 are conducting while diodes D1 and D3 are reverse biased. C2 and L2 are still being charged, while C3 and L3 are discharging in load R2.

The circuit of operation mode **d3** is shown in Fig. 3c. In this mode, both switches are turned off; diodes D1 and D2 are reverse biased while diodes D3 and D4 are conducting. Load R1 is being supplied by C2 and L2 while load R2 is supplied by C3 and L3.

In modes **d1** and **d2**, the tank circuit consisting of L1 and C1 works on filtering the signal going to output V1, while in **d3** it stops functioning.

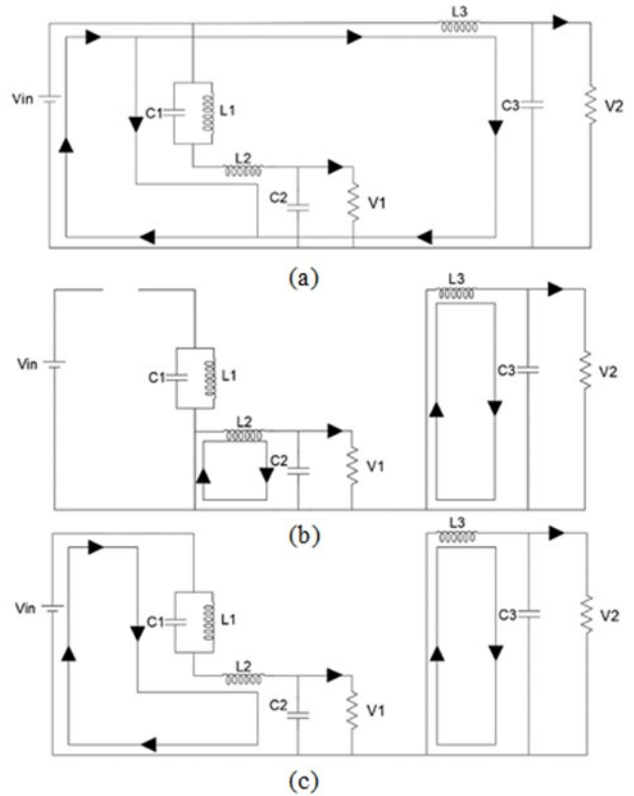


Fig. 3. he circuit of the proposed topology in the 3 modes of operation: (a) operation mode d1, (b) operation mode d2, and (c) operation mode d3.

2.2. Mathematical Modeling

In this section the average state space model will be derived based on the three modes of operation. The state variable will be considered as shown in Table 2. There will be only one input which is the input voltage and the outputs to be considered are V1 and V2. The general state space model of any system consists of four matrices A, B, C and D that determine the dynamic behavior and the input output relations in a system. The state space representation of a system is given in equation (1).

$$\begin{aligned} x' &= Ax + Bu \\ y &= Cx + Du \end{aligned} \tag{1}$$

Table 2. State variables of the mathematical model

State Variable Name	Assigned Parameter
x1	L1 current: I_{L1}
x2	C1 voltage: V_{C1}
x3	L2 current: I_{L2}
x4	C2 voltage: V_{C2}
x5	L3 current: I_{L3}
x6	C3 voltage: V_{C3}
u	V_{in}
y1	V1
y2	V2

2.2.1. Mode d1

In operation mode **d1**, the dynamics of the circuit are given in equations 1-6. From these equations, matrices A1 and B1 which are the A and B matrices of operation mode **d1** can be deduced.

$$x1' = -\frac{r1}{L1}x1 + \frac{1}{L1}x2 \tag{2}$$

$$x2' = -\frac{1}{C1}x1 + \frac{1}{C1}x3 \tag{3}$$

$$x3' = -\frac{1}{L2}x2 - \frac{r2}{L2}x3 - \frac{1}{L2}x4 + \frac{1}{L2}u \tag{4}$$

$$x4' = \frac{1}{C2}x3 - \frac{1}{R1+C2}x4 \tag{5}$$

$$x5' = -\frac{r3}{L3}x5 - \frac{1}{L3}x6 + \frac{1}{L3}u \tag{6}$$

$$x6' = \frac{1}{C3}x5 - \frac{1}{R2+C3}x6 \tag{7}$$

$$A1 = \begin{bmatrix} -\frac{r1}{L1} & \frac{1}{L1} & 0 & 0 & 0 & 0 \\ -\frac{1}{C1} & 0 & \frac{1}{C1} & 0 & 0 & 0 \\ 0 & -\frac{1}{L2} & -\frac{r2}{L2} & -\frac{1}{L2} & 0 & 0 \\ 0 & 0 & \frac{1}{C2} & -\frac{1}{R1+C2} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{r3}{L3} & -\frac{1}{L3} \\ 0 & 0 & 0 & 0 & \frac{1}{C3} & -\frac{1}{R2+C3} \end{bmatrix} \tag{8}$$

$$A2 = \begin{bmatrix} -\frac{r1}{L1} & \frac{1}{L1} & 0 & 0 & 0 & 0 \\ -\frac{1}{C1} & 0 & \frac{1}{C1} & 0 & 0 & 0 \\ 0 & -\frac{1}{L2} & -\frac{r2}{L2} & -\frac{1}{L2} & 0 & 0 \\ 0 & 0 & \frac{1}{C2} & -\frac{1}{R1+C2} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{r3}{L3} & -\frac{1}{L3} \\ 0 & 0 & 0 & 0 & \frac{1}{C3} & -\frac{1}{R2+C3} \end{bmatrix} \tag{16}$$

$$B1 = \begin{bmatrix} 0 \\ 0 \\ \frac{1}{L2} \\ 0 \\ \frac{1}{L3} \\ 0 \end{bmatrix} \tag{9}$$

2.2.2. Mode d2

In mode **d2**, equations 10 to 15 represent the dynamics of the proposed circuit and the matrices A2 and B2 are derived from those equations and given in equations 16 and 17 respectively.

$$x1' = -\frac{r1}{L1}x1 + \frac{1}{L1}x2 \tag{10}$$

$$x2' = -\frac{1}{C1}x1 + \frac{1}{C1}x3 \tag{11}$$

$$x3' = -\frac{1}{L2}x2 - \frac{r2}{L2}x3 - \frac{1}{L2}x4 + \frac{1}{L2}u \tag{12}$$

$$x4' = \frac{1}{C2}x3 - \frac{1}{R1+C2}x4 \tag{13}$$

$$x5' = -\frac{r3}{L3}x5 - \frac{1}{L3}x6 \tag{14}$$

$$x6' = \frac{1}{C3}x5 - \frac{1}{R2+C3}x6 \tag{15}$$

$$B2 = \begin{bmatrix} 0 \\ 0 \\ \frac{1}{L2} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{17}$$

2.2.3. Mode d3

The dynamics of the last mode of operation are given in equations 18 to 23, from which the matrices A3 and B3 are derived and given in equations 24 and 25.

$$x1' = -\frac{r1}{L1}x1 + \frac{1}{L1}x2 \tag{18}$$

$$x2' = -\frac{1}{C1}x1 \tag{19}$$

$$x3' = -\frac{r2}{L2}x3 - \frac{1}{L2}x4 \tag{20}$$

$$x4' = \frac{1}{C2}x3 - \frac{1}{R1*C2}x4 \tag{21}$$

$$x5' = -\frac{r3}{L3}x5 - \frac{1}{L3}x6 \tag{22}$$

$$x6' = \frac{1}{C3}x5 - \frac{1}{R2*C3}x6 \tag{23}$$

$$A3 = \begin{bmatrix} -\frac{r1}{L1} & \frac{1}{L1} & 0 & 0 & 0 & 0 \\ -\frac{1}{C1} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{r2}{L2} & -\frac{1}{L2} & 0 & 0 \\ 0 & 0 & \frac{1}{C2} & -\frac{1}{R1*C2} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{r3}{L3} & -\frac{1}{L3} \\ 0 & 0 & 0 & 0 & \frac{1}{C3} & -\frac{1}{R2*C3} \end{bmatrix} \tag{24}$$

$$B3 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{25}$$

2.2.4. Average model

First, it should be noted that the C and D matrices are the same for the three modes of operation and are given in equations 26 and 27 respectively.

$$C = \begin{bmatrix} 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{26}$$

$$D = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{27}$$

3. Simulation

The simulation of the proposed circuit was carried out using the MATLAB/Simulink software due to the ease of use and the accuracy of its results. The parameters of the circuit are given in Table 3. For the simulation of the proposed circuit, 2 sets of values will be taken into consideration, the

As for the A and B matrices of the whole system, they are going to be averaged based on the duty cycle of the system, hence:

$$A=A1.d1+A2.d2+A3.d3 \tag{28}$$

$$B=B1.d1+B2.d2+B3.d3 \tag{29}$$

The final A and B matrices are given in equations 30 and 31 respectively.

$$A = \begin{bmatrix} -\frac{r1}{L1} & \frac{1}{L1} & 0 & 0 & 0 & 0 \\ -\frac{1}{C1} & 0 & \frac{d1+d2}{C1} & 0 & 0 & 0 \\ 0 & -\frac{d1+d2}{L2} & -\frac{r2}{L2} & -\frac{1}{L2} & 0 & 0 \\ 0 & 0 & \frac{1}{C2} & -\frac{1}{R1*C2} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{r3}{L3} & -\frac{1}{L3} \\ 0 & 0 & 0 & 0 & \frac{1}{C3} & -\frac{1}{R2*C3} \end{bmatrix} \tag{30}$$

$$B = \begin{bmatrix} 0 \\ 0 \\ \frac{d1+d2}{L2} \\ 0 \\ \frac{d1}{L3} \\ 0 \end{bmatrix} \tag{31}$$

Figure 4 shows the response of the mathematical model in open loop operation with an input of 48V and desired outputs of 12V and 5V. It can be seen from the model response that V1 and V2 stabilize at 12V and 5V respectively showing that this model represents the circuit with accuracy.

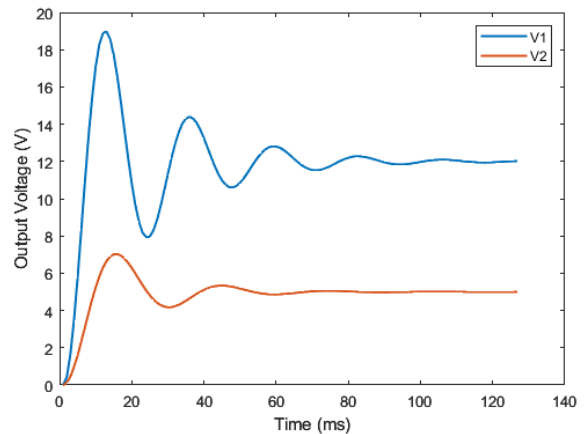


Fig. 4. Response of the mathematical model

first set will be used for comparing our topology with the one used in [28] and the other set will be based on the converters usually used in solar system applications. The parameters of the circuit for the first set are given in Table 3, while the outputs of the circuit are given in Table 4. Proportional-integral (PI) control will be used in this simulation to show that this circuit can function properly even with the simplest

control methods. The circuit of the simulated circuit is given in Fig.5.

Table 3. Parameters of the simulated circuit

Parameters	Values
Input voltage V_{in}	48V
Switching frequency of switch Q1 f_1	50kHz
Switching frequency of switch Q2 f_2	100kHz
Capacitor C1	0.5 μ F
Inductor L1	5 μ H
L1 resistance r1	0.01 Ω
Capacitor C2	3300 μ F
Inductor L2	1mH
L2 resistance r2	0.01 Ω
Capacitor C3	10000 μ F
Inductor L3	2mH
L3 resistance r3	0.01 Ω

Table 4. Output parameters of the simulated circuit

Outputs	Values
V1	12V
V2	5V
Current at V1: I1	6A
Current at V2: I2	5A
Output Power	97w

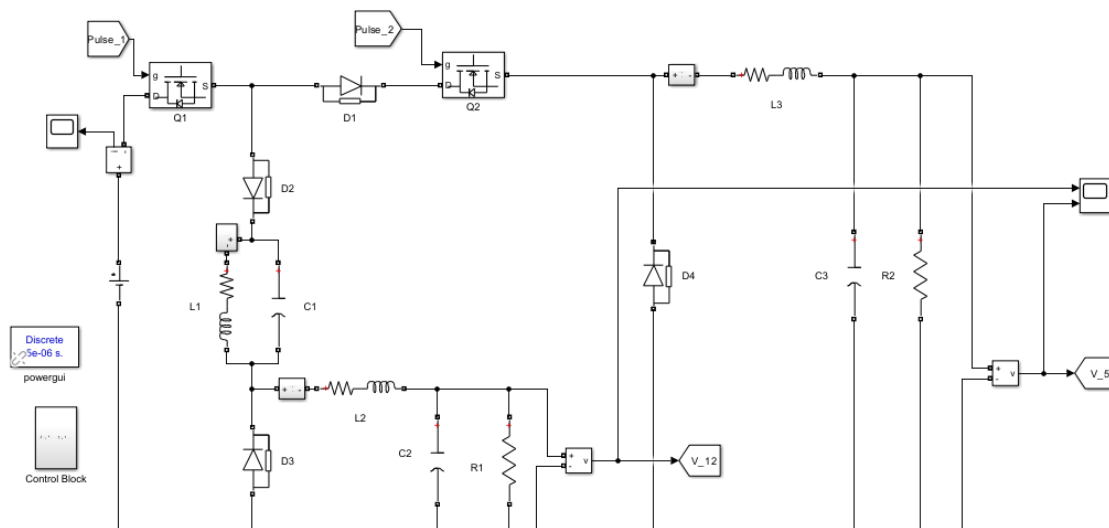


Fig. 5. The simulated circuit

Figure 6 shows the output voltage waveform of the circuit. It shows that this topology can output the two required voltage levels while supplying the required load. For the 12V output, the ripple factor was 1.83% while the percentage overshoot was limited to 42% and a settling time to 25ms. The 5V output as well has a ripple factor of 3%, a percentage overshoot of 30% and a settling time of 40ms. These results show that the proposed topology has both excellent transient and steady-state behaviors, maintaining a good balance between the overshoot and settling time while giving accurate low ripple outputs.

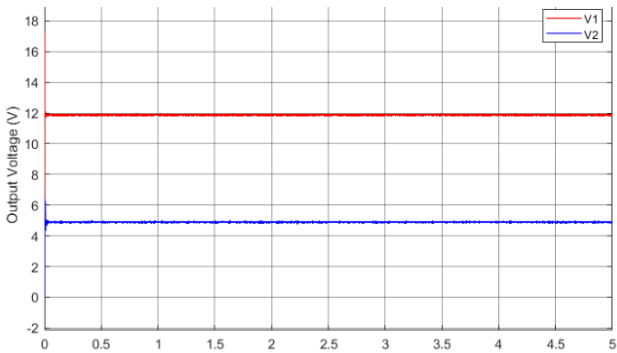


Fig. 6. Output voltage of the circuit.

Figures 7 and 8 show the current waveforms in inductors L2 and L3 respectively. These figures show that both outputs are functioning in continuous conduction mode (CCM) with inductor ripple current of 4A avoiding the disadvantages that come with discontinuous conduction mode (DCM) operation. Figure 8 shows 2 peaks per cycle, this is due to the different frequencies used in the circuit. And it is visible that these spikes take the form of steps before reaching a maximum value which stays within safe limits, which means that these spikes are not harmful to the circuit. Figures 9 and 10 show the current in inductor L1 and the voltage in capacitor C2 respectively. These figures show that the vales of the capacitor voltage and inductor current are varying (representing **d1** and **d2**) before stabilizing at zero (representing **d3**); this shows that the band-stop filter is filtering the unwanted frequency and then it stops functioning when it is no more needed. The efficiency of the circuit was calculated based on the simulation results which yielded a high value of 93.27%. This shows that not only does this circuit solve the problems previously stated, but also maintains an efficient performance while doing so. To understand the importance of adding the band-stop filter, the proposed topology will be compared with another topology found in literature. The topology used for comparison is introduced in [28], because the circuit proposed in [28] is very similar to the proposed circuit with the difference that the circuit in [28] does not contain the

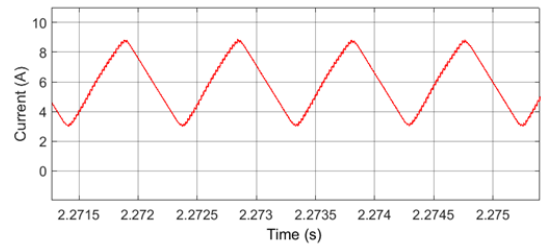


Fig. 7. Current in inductor L2.

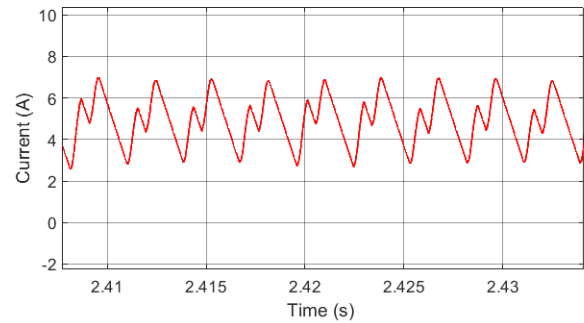


Fig. 8. Current in inductor L3.

tank circuit. The circuit introduced in [28] is shown in Fig. 11.

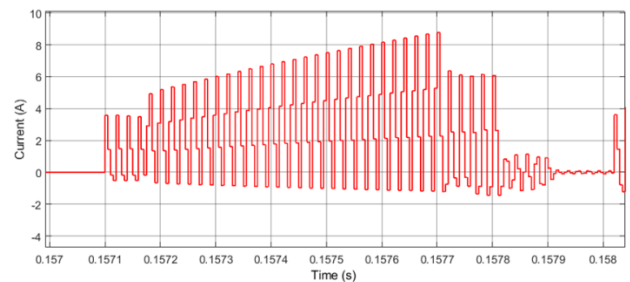


Fig. 9. Current in Inductor L1.

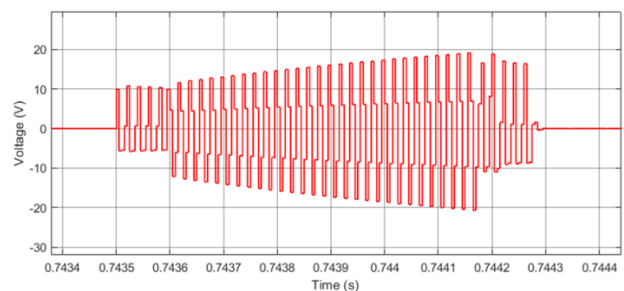


Fig. 10. Voltage in capacitor C1.

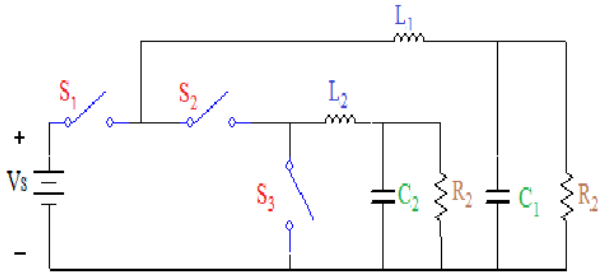


Fig. 11. Circuit of the topology introduced in [28].

The circuit from reference [28] was simulated with the same parameters and input and output voltages and currents, as the proposed topology. The output voltages of the circuit proposed in [28] are given in Fig. 12. The output voltage ripple factor for the 12V and 5V outputs were 1.83% and 3% respectively, and by looking at Fig. 12, the ripple factor of the 12V output from the topology in [28] is 3% while the ripple factor of the 5V output is 14%. So, it can be seen that the presence of the band stop filter and the use of different frequencies for the switches has decreased the ripple factor by a factor of 1.64 for the 12V output and a factor of 4.67 for the 5V output.

even though no change was applied to its part of the circuit, indicating an interference between the two outputs. However, in the proposed topology the ripple factor of the 5V output remained 3%, the same as before applying any changes, this proves the effectiveness of the band-stop filter in preventing the interference between the two outputs.

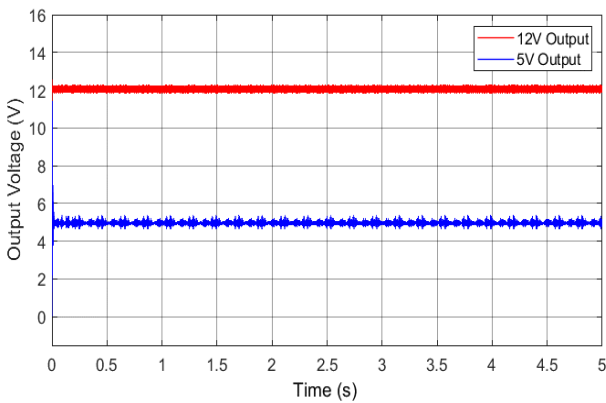


Fig. 12. The output voltages of the circuit proposed in [22] after changing the capacitor.

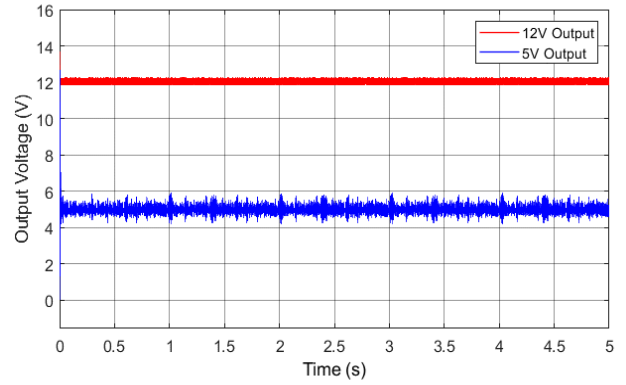


Fig. 13. The output voltages of the circuit proposed.

To understand the importance of the band-stop filter in preventing the interference between the outputs, the filtering capacitor connected in parallel to the 12V output of both circuits will be increased by a factor of three. The output of the circuit proposed in [28] is given in Fig. 12, while the output of the proposed topology is given in Fig. 13. By comparing the two outputs, the ripples in the 5V output in the circuit proposed in [28] have increased from 14% to 32%

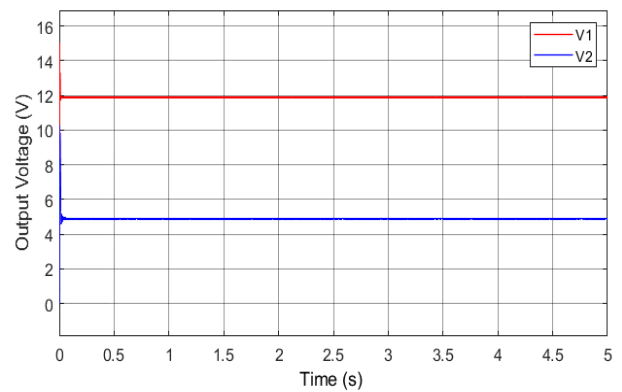


Fig. 14. The output voltages of the proposed circuit after changing the capacitor.

A third simulation was carried out based on the second set of values, to show the applicability of the proposed circuit in renewable energy applications. For that, the input voltage will be increased [29], same goes for the output voltages, load currents, the output power, and the different parameters of the circuit. The new parameters of the circuit and the output parameters are given in Tables 5 and Table 6 respectively.

Table 5. Parameters of the simulated circuit

Parameters	Values
Input voltage V_{in}	400V
Switching frequency of switch Q1 f_1	50kHz
Switching frequency of switch Q2 f_2	100kHz
Capacitor C1	1 μ F
Inductor L1	2.5 μ H
L1 resistance r_1	0.01 Ω
Capacitor C2	10000 μ F
Inductor L2	0.1mH
L2 resistance r_2	0.01 Ω
Capacitor C3	3300 μ F
Inductor L3	3mH
L3 resistance r_3	0.01 Ω

Table 6. Output parameters of the simulated circuit

Outputs	Values
V1	48V
V2	12V
Current at V1: I1	48A
Current at V2: I2	12A
Output Power	2.448Kw

It is important to note that the parameters for the input and output voltages as well as the load currents were chosen based on the ratings of conventional renewable energy appliances, mainly the solar charge controller [29-30].

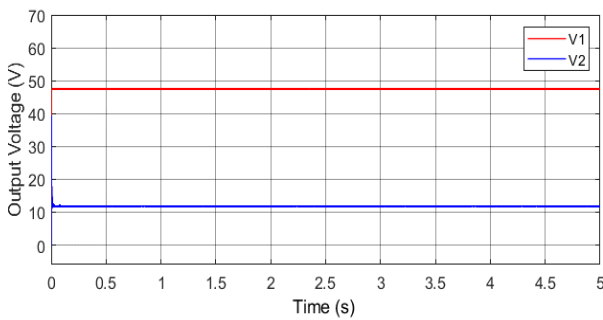


Fig. 15. The output voltage of the circuit for higher voltage and load current

Figure 14 shows the output voltage for the proposed circuit while handling high power and voltage. Figure 15 shows that the proposed topology can handle working with high voltages and supply considerable loads, all while maintaining a stable output with low ripple factor of 0.2% for the 48V output and 2.5% for the 12V output, all this while maintaining the main goal of isolating the outputs. Add to this that even with the increased load and the large difference between input and the output voltage levels, the converter still maintained a high efficiency of 90%.

4. Conclusion

In this paper, a new topology for SIDO buck converters was introduced. This converter was studied and modelled in state space. MATLAB/Simulink software was used to simulate the proposed circuit where it showed great transient and steady-state performance. Two simulations were carried out to show the functionality of this topology in low and moderate power renewable energy applications. The first simulation minimized the ripple factor from 3% to 1.83% for the 12V output and 14% to 3% for the 5V output with an efficiency of 93.27%. The second higher power simulation yielded even lower ripple factors with 0.2% for the 48V output and 2.5% for the 12V output while maintaining an efficiency of 90%. This topology was compared with another similar one found in literature, where it provided superior performance in terms of output ripple and isolation. As for future work, improvements can be made to this topology like adding more isolation to the lower voltage branch, improving the power handling capabilities to handle industrial level applications.

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